Threshold Voltage Improvement and Gate Leakage Current Reduction in a Multi-dot Room Temperature Operating Single Electron Transistor (RT-SET)

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ABSTARCT

The single-electron transistor (SET) is one of the best candidates for future nano electronic circuits because of its ultralow power consumption and small size. SET devices operate on the principle of Coulomb blockade, which is more prominent at dimensions of a few nano meters. Typically, the SET device consists of two capacitively coupled ultra small tunnel junctions with a nano island between them. The electron tunneling through the tunnel junctions can be controlled by the gate voltage. The drain current and the impact of the gate voltage depends on the overall capacitance of the device. Single electron transistors can be fabricated using methods like AFM nano oxidation, *e*-beam lithography, or shadow mask evaporation. Focused Ion Beam (FIB) based fabrication of SET devices is a novel method to produce SETs. The present paper describes the effect of additional series capacitance on the source-drain characteristic of a multi-dot room temperature operating SET device fabricated using FIB etch and deposition process. It also presents a novel method to minimize the gate leakage current and improve the threshold voltage in such multi-dot SET devices, operating at room temperature.

1. INTRODUCTION

SETs are a prime candidate for future nano scaled systems because of their low power consumption, smaller device area, their promising capability to integrate in ultra-high density memories, and their ability to sense minute charge fluctuations [Likharev et al. 1991]. The SET devices have device dimension in nano meter range and work in the principle of Coulomb blockade. Typically, the SET device consists of two capacitively coupled ultra small tunnel junctions with a nano island between them. However, the current transport can also be take place by multiple islands. Such kind of devices are called multi tunnel junction (MTJ) based SETs. The electron tunneling through the tunnel junctions can be controlled by the gate voltage.

SET devices have been fabricated using various technologies such e-beam evaporation [Y. Nakamura et al. 1996], metal deposition on prepatterned Si layer [Y. Takahashi et al. 1996], e-beam patterning on SIMOX layer and anodic oxidation by scanning probe microscope [J. Shirakashi et al. 1998]. However, the progress in fabricating room temperature operating single electron transistor (RT-SET) is slow. The greatest challenge is to fabricate the nano-island of size below 10nm, which is the critical dimension for a device to work at room temperature. Focused Ion Beam (FIB) based deposition technology is a novel technology to fabricate islands of that size and develop MTJ single electron transistors operating at room temperature [Karre et al. 2007]. The devices discuss in this paper are fabricated using FIB etch and deposition technology.

In a MTJ based SET device like ours, the current conduction takes place by tunneling of the electron through a series of junction in a single dominant conducting path (DCP). The current voltage characteristic and the performance parameters like threshold voltage (Vt) of the device depends on the capacitances associated with DCP. In this paper, we report the impact of additional series capacitances due to the additional nano-isands which do not participate in the current conduction process. A novel method to improve the threshold voltage and to reduce the gate leakage current is also presented.

2. EXPERIMENT

Fabrication Principle:-

Focused Ion Beam deposition and etching technology has been used for fabrication of multi island based single electron transistor. The devices were fabricated on a silicon substrate of dimension 0.5x0.5cm.The substrates were cleaned in a solution of H_2O_2 and H_2SO_4 (piranha solution) to remove any surface contaminants after which they were rinsed with de-ionized water and dried in nitrogen ambient. An Al_2O_3 thin film was deposited on the cleaned silicon substrate in a Perkin-Elmer 2400-8J parallel plate RF sputtering system. This film electrically isolates the devices from the substrate; the thickness of the film was 350nm. Subsequently a layer of Cr of was deposited in PE 2400 6'' RF sputtering system. This layer is the active layer in which the devices will be fabricated by further processing. The thickness of this active layer is set to be 20nm, which is the observed optimized thickness for highest resolution in our FIB

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14. ABSTRACT

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system. [Acharya et al. 2008]. Then the sample was introduced to HITACHI FB-2000A FIB system.

The device is formed in steps by using both etching and deposition technology in the FIB system. In the first step FIB etching technology was used to form the device pattern and hence isolating the active device from rest of the substrate. The dimension of each pads are 80x80µm and the length of the electrodes are 30micron. All the pattern transfer was made through the on-board software available in our FIB system. In the next step active area of the device was formed by trimming the source, drain and gate electrodes to 150nm each. Source, drain and gate gaps are formed by using an observation beam with a beam current of 1-4pA in vector scan milling mode. Controlling the dwell time and frame number (time of etching) in the vector scan fabrication mode, the desired dimension of the gap can be fabricated. A source drain gap of 17nm is achieved for dwell time of 30micro sec and frame number of 70; similarly a dwell time of 60micro sec and frame number 100 was used to make a 50nm gate gap. In the final step previously developed, [Karre et al., 2007] FIB based deposition technology was used to fabricate sub-10nm tungsten nano islands. As the sources drain gap is less than 20nm only 1-2 dots are expected to be present in between them. The Scanning Electron Micrograph of the fabricated SET is shown in Fig. 1.

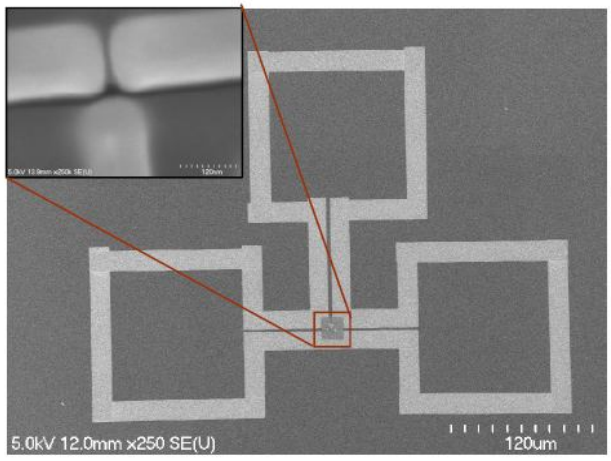

Fig. 1: SEM micrograph of the SET device The inset shows the active area of the device.

The fabrication of the quantum islands requires a deposition over the entire active area; contrary to the ideal condition of dots present only between source and drain terminals. A pictorial view of such a distribution is shown in Fig. 2. In such a multi-dot SET device, the electron tunneling occurs through a single dominant path [A.S.Cordan et al.] hence, only few numbers of dots take part in the current conduction whereas the majority of the remaining dots are non-participating. To study the impact of these non-participating dots on the V-I characteristic of the device, two different set of device are formed. For one of these two sets of devices the additional dots are removed by FIB etching process as shown in Fig. 3. In the other hand for the other SET of devices the additional dots are present. The removal of these dots is done using MO50 beam in our FIB system in raster scan mode.

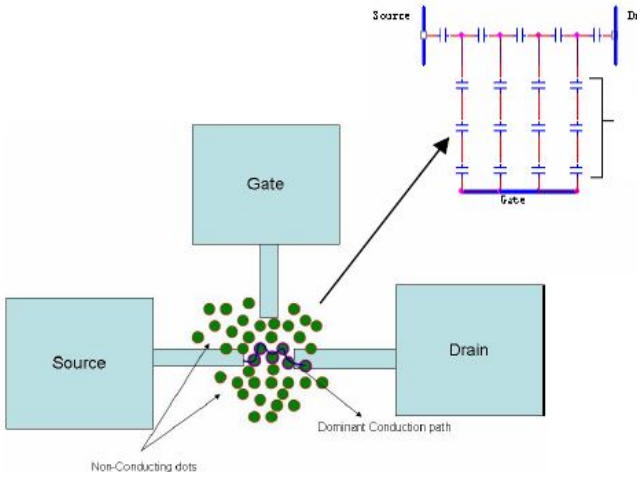

Fig. 2: Pictorial view of a fabricated device with additional non-participating dots. The inset represents an approximated model of such a device.

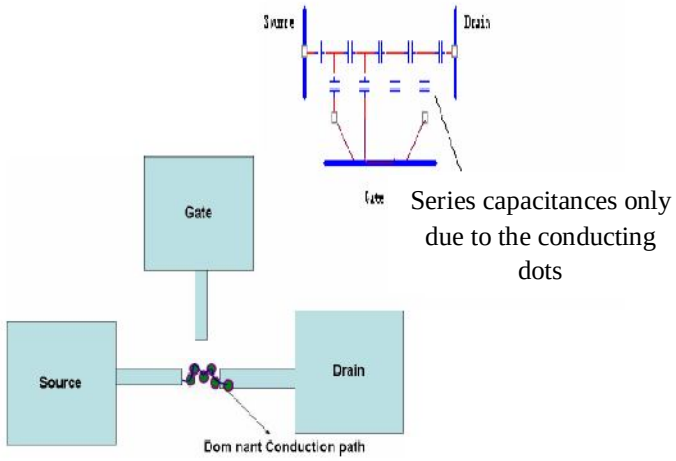

Fig. 3: Pictorial view of a SET device without additional non-participating dots. The inset represents an approximated model of such a device.

The tungsten nano islands were oxidized by peracetic acid, which is a combination of acetic acid and H_2O_2 in the ratio 1:1, by volume, for 2 mins. peracetic acid, being a strong oxidizing agent, oxidizes the surface of the tungsten nanoparticles forming a thin layer of tungsten oxide. This oxidation was done to form the

tunnel junction for the SET. Now the active device is formed. After subsequent cleaning and rinsing process in de-ionized water, a 30nm Al_2O_3 thin film was deposited on the substrate as a passivating layer. Finally, the probing pads were exposed by etching the passivating Al_2O_3 layer, using FIB milling process.

3. RESULTS AND DISCUSSION

The devices are tested in a room temperature ambient using Keithley 4200-SCS semiconductor parametric analyzer (SPA). A micromanipulator probe station is used to probe the device pads. The change in current with a voltage sweep from –7 to 7 volts, for the two set of the devices are obtain for a constant gate voltage of 50mV as shown in Fig. 4. The solid blue line in Fig. 4 represents the V-I characteristic of the device with non-conducting dots and the plot with red dots represents the V-I characteristic of the device without the non-participating dots.

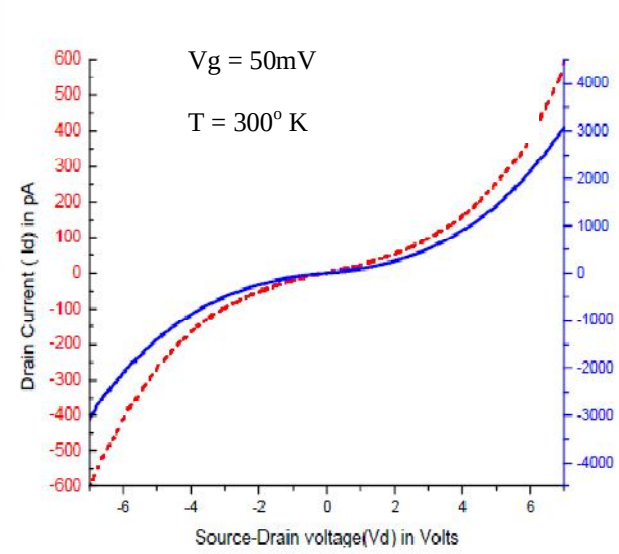

Fig. 4: Room temperature V-I characteristics of the SET devices with and without the non-participating dots.

Clear Coulomb blockade is observed in both set of devices. However, the threshold voltages and hence the blockade length for these devices are different. This fact will be explained in detail in the next section. In addition to the source drain characteristic, the gate leakage current with respect to the source drain voltage is also measured for both the set of the devices.

Analysis:-

Threshold voltage of a SET can be defines as the voltage at which the device transit from blockade state to non-blockade state. Quantitatively it is half of the blockade length for a certain gate voltage and the blockade length could be directly related to the charging energy of the device. From the V-I characteristic of our fabricated device in Fig. 4, it can be observed that the threshold voltage for a device without any non-participating dots is smaller than that of a device with non-participating dots. In other words, the blockade length of the SET device decreases if the non-participating dots are removed from the active area. This fact could be analyzed by using capacitance analysis.

The charging energy Ec for a SET device could be expressed as Eqn.1.

$$Ec = e^2/2C_{eff} \ldots\ldots\ldots \text{Eq.1}$$

Where E_c= *Charging Energy*

$$e = Electronic\ Charge$$

$$C_{eff} = total\ effective\ capacitance\ of\ the\ Dots$$

For a multi-dot based SET device the total effective capacitance C_{eff} consists of the intra dot capacitance in the DCP (dominant conducting path), capacitances associated due to the electrode terminals, and the additional capacitances associated due to non-participating dots. Figure 2 and 3 shows the pictorial views of the SET devices, with the capacitance associated due to various structures.

It could be observed that, for a device with additional non-participating dots, the number of series capacitances associated with the DCP is higher than that for a device without any non-participating dots. These series capacitances decrease the total effective capacitance of the device and hence increase the threshold voltage (Eq.1). Therefore by removing the non-participating dots, these series capacitances could be eliminated and hence the threshold voltage could be improved. This fact could be observed from the capacitance model of the device as shown in Fig. 2 and 3, and the decrease in the threshold voltage could be observed in Fig. 4.

In addition to the threshold voltage improvement, removal of these non-participating dots from the active area also has impact on the gate leakage current. The gate leakage current with respect to the source drain voltage for the devices with non-participating dots are shown in Fig. 5a . From the blockade nature of the gate current characteristic as shown in Fig. 5a, it could be expected that, the gate leakage current is basically from the unintended tunneling accruing from the source terminal to the gate terminal through the non-participating dots.

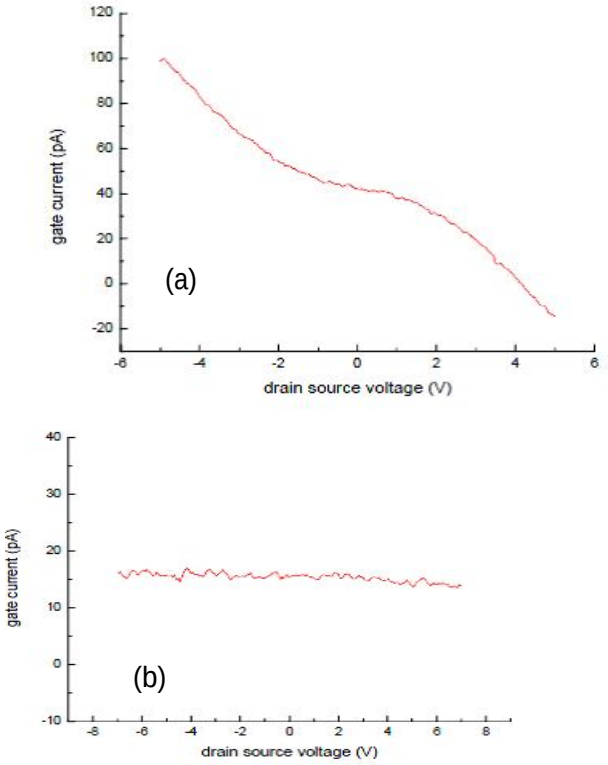

Fig. 5: Plot showing the gate current with respect to the source-drain voltage in a multi dot RT-SET (top) with and (bottom) without non-participating additional dots.

Therefore, removing these dots the leakage current could be minimized. This is validated by measuring the gate current for a device in which the non-participating dots are removed and plotted in Fig. 5b. Comparing these two characteristics it can be observed that the gate leakage current is decreased by two orders of magnitude in a device without the additional non-participating dots. Removing the non-participating dots blocks the path for tunneling and hence decreases the leakage current.

4. CONCLUSION

Focused Ion Beam based etch and deposition technology has been used to fabricated MTJ based SETs operating at room temperature. The current conduction takes place in a dominant conducting path in a MTJ based device. The additional non-participating dots increases the series capacitances associated with DCP. The device functionality can be improved by eliminating these removing the non-participating dots. When these non-participating dots are removed by FIB etching process, a substantial improvement in the threshold voltage is achieved. Also, the removal of these additional dots resulted in a reduction in gate current by two orders of magnitude.

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